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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/037,366	01/04/2002	Steven Turner	1376.0200130	6465

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EXAMINER	
NGUYEN, HAU H	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/037,366	Applicant(s) TURNER ET AL.	
	Examiner Hau H Nguyen	Art Unit 2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05/27/2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) *2* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Arguments

1. Applicant's arguments with respect to claims 1, 3-29 have been considered but are moot in view of the new grounds of rejection.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 13-26, and 29 are rejected under 35 U.S.C. 102(b) as being anticipated by Kou (U.S. Patent No. 5,874,928).

Referring to claims 13, 14, 17, Kou teaches a display controller 16 the operation of which is shown in Fig. 4 with reference to Fig 2. The serialized data stream is outputted (step 112) to the first converter 42, preferably at a rate determined by the video clock signal. In response, the first converter 42 converts 116 the serial data stream into a first set of video signals having both an analog portion and a digital portion (receiving a first set and a second set of graphics data). The analog portion is sent 120 on to the CRT display to drive the display (to an external graphics controller, for example the CRT controller 58, Fig. 2), while the digital portion is processed further. As shown in FIG. 2, the analog portion of the video signals are sent to the display at a rate determined by the rate of the video clock signal. Preferably, the rate of the video clock signal is selected such that it causes the refresh rate of the CRT display to be optimized. This ensures that the CRT display will operate at its optimal level. The first display is thus driven.

To drive the second display, the digital portion of the first set of video signals needs to be converted into a second set of video signals, which can be used to drive the second display. This conversion process preferably begins with processing (step 124) the digital portion of the first set of video signals through the second converter 44 to generate a second stream of graphics data, which is appropriate for display by the second display (the LCD). The dithering engine 54 thereafter converts 144 the stream of graphics data from the read buffer 50 into a second set of video signals, and sends 148 the video signals to the flat panel controller 56 (liquid crystal display controller). Finally, the controller 56 sends 152 the video signals to the LCD (to an external display interface) at a rate determined by the rate of the memory clock signal. The second display is thus driven (col., lines). The examiner makes the assumption that the components 42, 44, 45, 50, 54, and 56 (Fig. 2) together is the graphics controller, the frame buffer controller 52 is the memory controller since on column 8, lines 52-57, Kou teaches if so desired, display memory 36 and frame buffer 48 may be implemented using a single memory (system memory), with the display memory 36 and the frame buffer 48 being separate partitions or portions of the memory.

In regard to claim 15, 16, 18, and 19, Kou teach a host computer 12 (Fig. 1), which may be any desired type of computer, such as a Personal Computer, generates, updates, and provides graphics data to the display controller 16. It is the responsibility of the display controller 16 to convert the graphics data stored in display memory into video signals that can be used to drive the displays 18a-n. In general, there may be any number of displays 18a-18n, and the type of display may vary. In the preferred embodiment, there are two displays, with one display being a CRT display and the other display being an LCD (col. 5, lines 1-11). Thus, it is implied that in

case where the computer is a laptop computer (portable device), the display is an integrated liquid crystal display, and the CRT display is a remote display. The converters format the first and second sets of data for the appropriate display device is cited above.

Referring to claim 20, Kou teaches the CRT controller 58 is the component responsible for generating the control signals, and controlling the overall operation of the display (col. 7, lines 40-47).

In regard claims 21-23, 25, and 29, Kou teaches the display controller 16 of FIG. 2 may take one of many forms. It may be implemented in the form of a single integrated circuit device, or it may be implemented with several discrete components on a printed circuit board (col., lines). As cited above, the display controller 16 receives a first and second set of graphics data, wherein the first set of graphics data is provided to an integrated display device (for example a LCD display in a laptop computer), and a second set of graphics data is provided to a display interface of a remote display (a CRT display, Figs. 1 and 2).

Referring to claim 24, Kou teaches the color LCD display panels in current products generally fall into two basic types--active matrix and passive matrix. In the active matrix display panel, a trio of thin film transistors (TFT) is paired with liquid crystal elements to activate each pixel (col. 1, lines 28-32).

In regard to claim 26, Kou teaches the video controller 32 preferably comprises a sequencer and a graphics controller. The sequencer is primarily responsible for controlling the flow of data between the host computer 12 and the display memory 36 via bus 14 according to the mode (such as EGA, VGA, etc.) set for the controller 16 (col. 5, lines 52-62). Thus, it is implied that the remote display should includes a video graphics adapter display.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 3-8, 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kou (U.S. Patent No. 5,874,928) in view of Reddy et al. (U.S. Patent No. 6,075,513).

Referring to claims 1, 4, 6, 7, and 11, as cited above, Kou teaches an embedded graphics controller (components 42, 44, 45, 50, 54, and 56, Fig. 2) to generate a first rendered graphics data to be displayed on an LCD display device, an embedded display interface (first converter 42, Fig. 2) to format a second rendered graphics data to output to a remote display (CRT display). As shown in Fig. 1, the display controller 16 can also couple to a plurality of display devices 18a-18n (col. 5, lines 4-10), and thus can coupled to a second remote display device. Kou further teaches together, components 30, 32, 34, and 36 interact with the host computer 12 to receive, manipulate, and store the graphics data generated by the host computer 12. In converting the graphics data stored in the display memory 36 into a set of video signals appropriate for driving a CRT type of display, the video buffer 38, the data serializer 40, and the first converter 42 are used (col. 6, lines 19-34). Thus, components 30-36 (display controller) are used to generate a second rendered graphics data and provide to the converter 42 (display interface)

Thus, Kou teach all the limitations of claims 1, 4, 6, and 7, except that the display controller is interfacing a system on chip having a first interface and second interface.

However, as shown in Fig. 4A, Reddy et al. teach a computer system 150, comprising a system on chip 120, having a first interface 430, and a second interface 401. Reddy et al. further teach an embedded graphics controller 126 that can support a panel display 132 or an external cathode ray tube (CRT) display 103 (col. 1, lines 18-22). As shown in Fig. 4A, the graphics controller 126 can generate a first graphics data to be displayed on an integrated display 112, and a second graphics data to be displayed on a remote display 103.

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Kou in combination with the method as taught by Reddy et al. so that the display image can be improved as operating conditions change, and few changes are required to the existing interface architecture (col. 3, lines 6-13).

In regard to claim 3, as cited above, Kou teach the graphics controller receives non-rendered graphics data, and rendered graphics data in order to be displayed on the LCD display device.

Referring to claim 5, although not explicitly stated, it is inherent that the display interface (first converter 42) as taught by Kou, should receive control signals from the graphics controller in order to properly display on the CRT display since there are cases when the display controller 16 can simultaneously drive both LCD and CRT displays (col. 6, lines 24-30, and col. 7, lines 39-47).

In regard to claim 8, Kou teaches the video controller 32 preferably comprises a sequencer and a graphics controller. The sequencer is primarily responsible for controlling the

flow of data between the host computer 12 and the display memory 36 via bus 14 according to the mode (such as EGA, VGA, etc.) set for the controller 16 (col. 5, lines 52-62). Thus, it is implied that the remote display should includes a video graphics adapter display.

In regard to claim 12, Kou teach the display controller 16 preferably further comprises a power controller 60 coupled to the display memory 36. The function of controller 60 is to turn off selected components when these components are not needed, and there may be occasions where: only the LCD is being driven (col. 9, lines 53-61). Thus, in this case, the display interface is disabled to conserve power.

6. Claims 27-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kou (U.S. Patent No. 5,874,928) in view of Narui et al. (U.S. Patent No. 6313813).

Referring to claims 27-28, as applied to claim 1 above, Kou teach all the limitations of claims 27-28, except for the display interface includes a Transition Minimized Differential Signaling output interface or a Low Voltage Differential Signaling output interface.

However, Narui et al. teach a converter resides in the monitor having display signals transmitted by the PC to the monitor in digital form. A receiver is incorporated as part of the display data input of the monitor and receives the digital display signals and forwards them to the converter. In the preferred embodiments, the receiver is one of a transition-minimized differential scaling (TMDS) receiver, a low voltage differential signaling (LVDS) receiver (col. 2, lines 62-67, and col. 3, lines 1-5).

Therefore, it would have been obvious to one skilled in the art to utilize the method of receiving different input signals for a display as taught by Narui et al. in combination with the

graphics system as taught by Kou in order to allow the display devices having display circuits that output display signals at a variety of different scanning frequencies and display resolutions (col. 1, lines 60-63).

7. Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kou (U.S. Patent No. 5,874,928) in view of Reddy et al. (U.S. Patent No. 6,075,513) and further in view of Narui et al. (U.S. Patent No. 6313813).

Referring to claims 9-10, as applied to claim 1 above, Kou and Reddy et al. teach all the limitations of claims 9-10, except for the display interface includes a Transition Minimized Differential Signaling output interface or a Low Voltage Differential Signaling output interface.

However, Narui et al. teach a converter resides in the monitor having display signals transmitted by the PC to the monitor in digital form. A receiver is incorporated as part of the display data input of the monitor and receives the digital display signals and forwards them to the converter. In the preferred embodiments, the receiver is one of a transition-minimized differential scaling (TMDS) receiver, a low voltage differential signaling (LVDS) receiver (col. 2, lines 62-67, and col. 3, lines 1-5).

Therefore, it would have been obvious to one skilled in the art to utilize the method of receiving different input signals for a display as taught by Narui et al. in combination with the graphics system as taught by Kou and Reddy et al. in order to allow the display devices having display circuits that output display signals at a variety of different scanning frequencies and display resolutions (col. 1, lines 60-63).

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 703-305-4104. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on 703-308-6829.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D. C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

H. Nguyen

08/02/2004

Matthew C. Bella

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